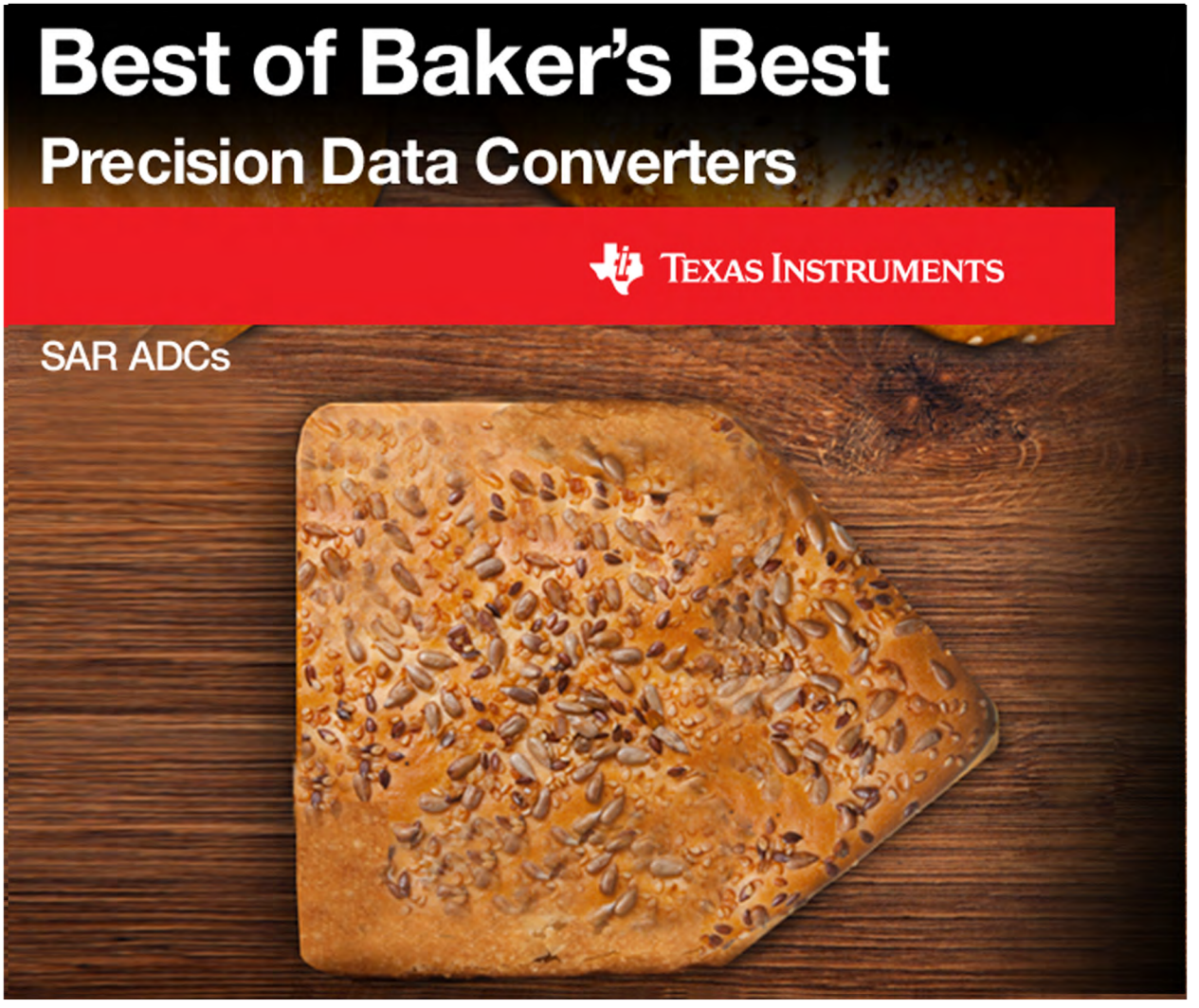

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Introduction by Bonnie Baker

Successive approximation register analog-to-digital converters (SAR ADCs) bridge the gap between the analog and digital domains in your medium-frequency, medium-accuracy circuits. SAR ADCs target the precision space where medium speed, millivolts, linearity and noise matter.

SAR ADCs have been around for a long time and for very good reasons. They are easy to use and, because of their innate ability to shut down between conversions, they lend themselves well to battery-powered applications.

The following excerpts from EDN's Baker's Best column represent the best of my SAR ADC short articles. They have been complied into this e-book for your convenience. Please enjoy and let me know what you think at ti_bonniebaker@list.ti.com!

P.S. Want to learn more about data converters? We have even more information about data converters on the TI website and the Precision Hub and Analog Wire blogs on the TI E2E™ Community site.

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1. What's in your SAR ADC application?

"Finding an amplifier that doesn't tarnish an ADC's performance is hard enough. But now you also have to deal with single-supply voltages and the quirky switched-capacitor input structure" (reference 1).

Engineers have been struggling with the task of driving the successive approximation register analog-to-digital converter (SAR ADC), charge redistribution or capacitive data-acquisition converter (C-DAC) input architectures for more than a decade.

Driving a SAR ADC with an amplifier seems like a simple task: You choose an amplifier with a bandwidth appropriate for the input-signal requirements, then connect the amplifier directly to the ADC as a buffer. Not so fast. You are not finished until you accommodate the effects of the ADC-input charge injection on your amplifier (Figure 1). The transient currents at the input of the SAR ADC can disrupt the output of the amplifier so that the conversion process produces inaccurate digital results.

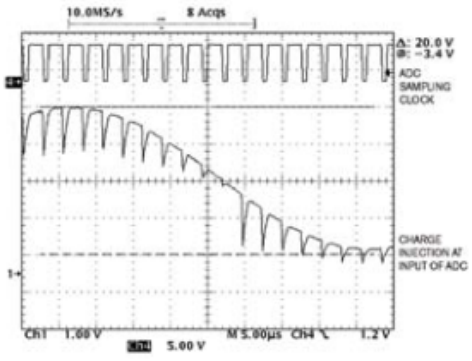

Figure 1: By placing a 10-kΩ resistor between a buffer operational amplifier (op amp) and a SAR ADC input, you can see the ADC charge-injection action.

Model the input structure of the SAR ADC with a switch to an input capacitor, C_{SH}, to ground (Figure 2). Before signal acquisition, the ADC S_2 switch connects the power supply, voltage reference or ground to pre-charge C_{SH}. Your particular ADC topology determines this pre-charged voltage value. At the start of the signal-acquisition time, S_2 opens and S_1 closes. When S_1 closes, the system injects charge onto or off of C_{SH}, and the ADC takes a pre-determined amount of time to acquire the signal. During this signal-acquisition time, the ADC requires ample charge from an input source to bring the system within a ½-LSB accuracy window.

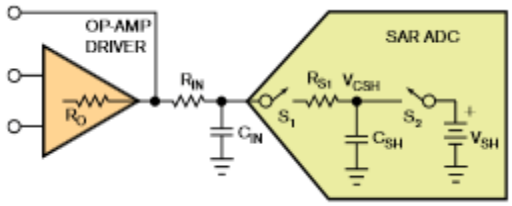

Figure 2: Choose an amplifier with an input range appropriate for the input-signal requirements; then connect the amplifier through a resistor/capacitor (RC) system to the ADC.

To design your circuit to perform accurately with the first pass, insert a resistor, R_{IN}, and a capacitor, C_{IN}, in the signal path between the amplifier and the ADC (Figure 2). The capacitor serves as a charge reservoir, providing ample charge to the input capacitor of the ADC. R_{IN} isolates the amplifier from C_{IN} and stabilizes the amplifier (Reference 2). The combination of R_{IN} and C_{IN} needs to at least meet the ADC's acquisition time (Reference 3). Finally, select your amplifier bandwidth to match the $R_{IN}C_{IN}$ time constant.

If you design your SAR ADC circuit by simply driving the input of the converter with an amplifier, it may not produce good results. If you insert an RC pair between the amplifier and the SAR ADC, you will successfully charge your converter and design the quirks out of your circuit from the start.

References

1. Swager, Anne Watson. Evolving ADCs demand more from drive amplifiers. EDN, September 29, 1994
2. Green, Tim, "Operational amplifier stability, Part 3 of 15: R_O and R_{OUT}," *Analog Zone*, 2005
3. Oljaca, Miro, and Bonnie Baker. Start with the right op amp when driving SAR ADCs. EDN: Oct 16, 2008

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2. Charge your SAR converter inputs

It is tempting to drive a successive approximation register analog-to-digital converter (SAR ADC) straight-on with an amplifier. As an added benefit, you might try to configure the amplifier circuit in a gain or anti-aliasing filter stage. These seem like reasonable enhancements as you try to optimize the use of your devices. However, did you think about whether you would compromise the effectiveness of your operational amplifier (op amp)/data converter pair (Figure 1)?

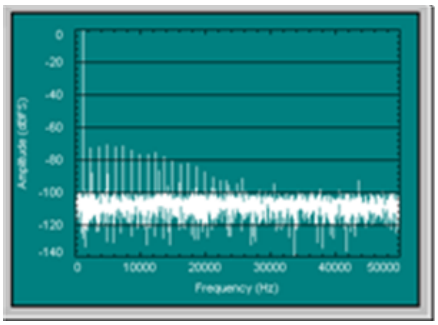

Figure 1: An improperly driven, 12-bit SAR ADC can produce unwanted noise and harmonic distortion. In this diagram, the signal-to-noise ratio (SNR) is 69.76 dB full scale, and the total harmonic distortion (THD) is 63.34 dB full scale for a converter that performs at an SNR of 71.82 dB full scale and a THD of 78.82 dB full scale.

If you need good, accurate performance (at DC as well as AC), regardless of your throughput rate, the analog input stage of the SAR ADC requires special attention. The model of the input stage of most modern ADCs is a resistor/capacitor (R/C) pair with two switches and a voltage source (Figure 2). The resistance, R_{SW}, in the input of the converter is the closed-switch resistance. This switch closes during the acquisition time of the conversion process and opens during the conversion time. The data converter uses capacitance, C_{SH}, which is the total of the distributed on-chip capacitance for the input-signal sampling process.

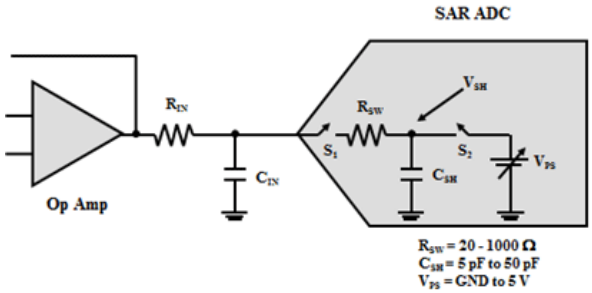

Figure 2: The input structure of a SAR ADC initially has a sample-and-hold capacitor, C_{SH}, following a switch, S1, which controls the sampling time.

First and foremost, you need to give the sample capacitor, C_{SH}, enough charging time to reach at least ½ LSB of final value. Theoretically, for a 12-bit SAR ADC, this would be more than eight times $R_{SW} * C_{SH}$. Given error margins and component variations, I recommend multiples of 10 to 15. The data converter needs an op amp in a gain of ±1 V/V along with an external R/C pair (R_{IN}, C_{IN}). During sampling, the ADC uses the capacitor, C_{IN}, for signal stability. The resistor, R_{IN}, isolates the amplifier from the load capacitance of the ADC. The op amp isolates the ADC from high-impedance loads as well as driving C_{IN} and C_{SH}, facilitating a quick charge time while the ADC is sampling.

You design this seemingly simple circuit with the following guidelines. C_{IN} is a silver mica or C0G dielectric-type capacitor. These types of capacitors provide stability to the voltage and frequency coefficient of C_{SH}. X7R, Z5U and other types of capacitors have significant voltage and frequency "memory" and might degrade the THD performance of the converter. The value of C_{IN} is, at minimum, greater than 20 times C_{SH}. You determine the value of R_{IN} using the ADC internal R/C values. The time constant of the final values of C_{IN} and R_{IN} is 70 percent of the C_{SH}/R_{SW} time constant, with a value of 50 $\Omega < R_{IN} < 2$ kΩ. Finally, the op amp circuit, with C_{IN} and R_{IN} installed, should be able to settle to your data converter's resolution while driving a step-response signal. It is appropriate to prove this function with bench testing.

Avoid the temptation to neglect the input-driving circuit of your SAR ADC. The plusses outweigh the minuses if you add a driver amplifier and an appropriate R/C pair at the ADC input. With this approach, you will drive your data converter to picture-perfect performance.

References

1. Baker, Bonnie. Matching the Noise Performance of the Operational Amplifier to the ADC. Texas Instruments Analog Applications Journal, 2Q06
2. Oljaca, Klein, Numberg. Optimizing the High Accuracy Measurement Circuit. 2004 PCIM Conference.

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3. Absorb current spikes and noise with a simple technique

When using an 8- to 14-bit analog-to-digital converter (ADC) in your system, it is critical that you understand the voltage-reference path to the data converter. Figure 1 shows a circuit that accommodates the dynamics of the ADC's reference input. In this figure, the voltage-reference chip provides a voltage foundation for the conversion process and a capacitor, C_{L1}, to absorb the ADC's internal reference circuitry current spikes and filter-reference noise (Reference 1). It is important not only to reduce voltage-reference noise in this circuit, but also to balance the stability of the internal voltage-reference amplifier.

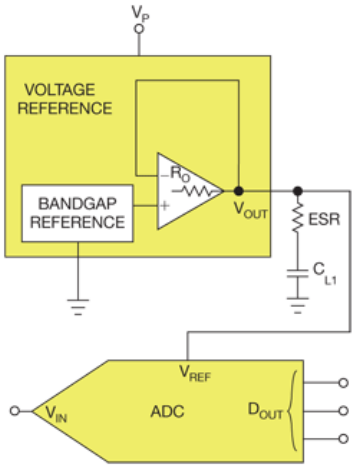

Figure 1: This circuit accommodates the dynamics of an 8- to 14-bit ADC's reference input.

When addressing the noise issue with this circuit, the ADC transfer function reveals the role of the voltage-reference noise expressed as Equation 1:

$$CODE=V_{IN}(2^N/V_{REF}) \quad (1)$$

where V_{IN} is the input voltage to the ADC, N is the number of ADC bits and V_{REF} is the reference voltage to the ADC.

The reference-voltage variable includes all errors associated with the reference chip, such as accuracy, temperature variations and noise. In all cases, reference errors become part of the gain error of the ADC system.

You can calibrate most of these errors with the system processor or controller. If measuring several points from the negative full scale to the positive full scale of your ADC, you will see a gain error from these errors as a function of the data converter's input voltage. Noise is one error that you cannot calibrate with your processor or controller. The reference noise at the output of the converter grows larger with the analog input voltage (Figure 2).

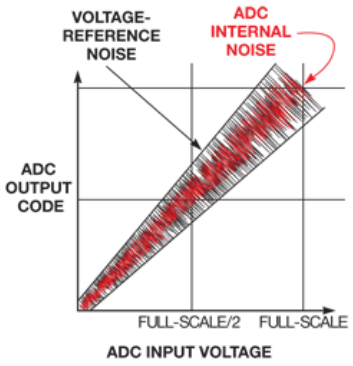

Figure 2: The reference noise at the output of the data converter grows larger with the analog input voltage.

Datasheets for most voltage references have an output-voltage noise specification over a 0.1- to 10-Hz frequency range. Some manufacturers include specifications for the voltage reference output-noise density. This specification usually refers to noise in the broadband region, such as the noise density at 10 kHz. Regardless of how the manufacturer specifies the noise of this reference, however, an added low-pass filter reduces overall noise at the reference output. You design this filter with a capacitor and the equivalent series resistance (ESR) of the capacitor. You ensure stability in the design by using the techniques recommended in Reference 2.

The accuracy of Figure 1's voltage reference is important; however, you can calibrate any initial inaccuracy with hardware or software. On the other hand, eliminating or reducing reference noise while absorbing the current spikes on the ADC's reference pin requires characterization and hardware-filtering techniques.

References

1. Baker, Bonnie. Taking the mixed-signal voltage reference to a higher level. EDN, September 23, 2010.

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4. ADC voltage-reference errors impact full-scale conversions

Successive-approximation-register (SAR) analog-to-digital references have more influence on conversion accuracy than you may initially think. Figure 1 shows the transfer function of an ideal 3-bit analog-to-digital converter (ADC) and the same data converter with gain error.

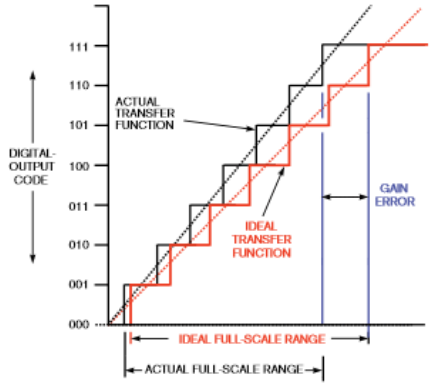

Figure 1: Gain error causes the transfer function of an ADC to rotate around the digital-input code of zero.

The transfer function of an ADC is equal to Equation 1:

$$D_{CODE} = (V_{IN} - V_{OS}) \left[\frac{2^N}{V_{REF} - V_{GE}} \right] \quad (1)$$

where D_{CODE} is the digital output code; V_{IN} is the input voltage to the converter; V_{OS} is the data converter's offset voltage; V_{REF} is the reference voltage applied to the data converter; N is the number of ADC bits or the ADC resolution; and V_{GE} is the combined ADC-gain error, reference-output-voltage error and reference-voltage noise.

It is easy to see how the voltage reference's specified value affects the ADC's absolute accuracy. For high-resolution data converters, the reference-offset error is usually greater than the ADC-offset error, particularly over temperature. You will also notice from the transfer function that the reference errors have more influence on the converter results with higher input voltages.

You can reduce the ADC and reference-source errors with a ratiometric design. This scenario may require additional devices in the circuit or a processor/microcontroller-calibration algorithm. Remember that calibration algorithms require gain and offset characterization for each circuit.

The reference's noise error is a different matter. It affects the signal-to-noise ratio (SNR) and the total harmonic distortion (THD) of a conversion. The reference noise impacts the converter's SNR and THD at higher ADC input voltages (Figure 2).

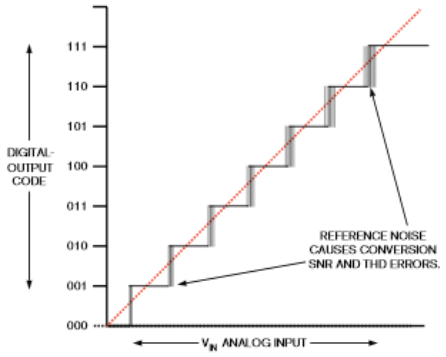

Figure 2: The voltage-reference noise of the ADC grows when output digital codes increase.

If the data converter lacks an internal buffer at the reference pin, you will notice incoming or outgoing current spikes. The data converter uses these currents during the conversion cycle to charge internal capacitors. This knowledge may motivate you to insert a low-noise amplifier between the external reference and the ADC.

Don't try to test your ADC with an input voltage of 0 V or ground. If you hope to see the effects of your voltage-reference source on your conversions, try to use a DC full-scale input and then a signal input that will help you look at the system's frequency response.

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5. Taking the mixed-signal voltage reference to a higher level

The voltage reference in a mixed-signal application can make or break a system (Reference 1). The greatest impact of a noisy or a marginally stable reference is at or near the data converter's full-scale output. You can improve this scenario by looking for the lowest-noise, most accurate, most-stable reference on the market, but you may want to try to take another approach. If cash flow is a little tight right now, a bit of design finesse can save the day.

First, consider the ins and outs of the data converter's reference-pin input. Figure 1 shows an example of the charge spikes that can appear on a modern analog-to-digital converter's (ADC) voltage-reference pin during a conversion. The top trace is the start-convert signal to the converter. The ADC's voltage-reference pin (bottom trace) demands different amounts of charge during the conversion. In this figure, an oscilloscope's low-capacitive probe captures the voltage drop across a 10-kΩ resistor between the input of the ADC voltage-reference pin and the voltage-reference output. The voltage reference for an ADC must be able to accommodate these high-frequency charge spikes.

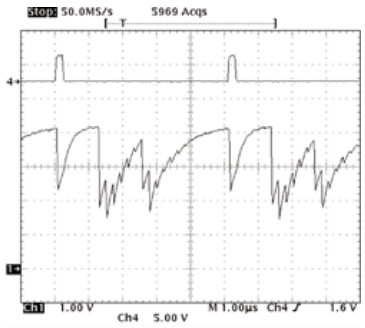

Figure 1: Charge spikes can appear on an ADC's voltage-reference pin during a conversion. The top trace represents the strobe that initiates a conversion. The ADC's voltage-reference pin (bottom trace) demands different amounts of charge during the conversion.

Voltage references are available in two-terminal shunt or three-terminal series configurations. The two-terminal shunt-voltage reference implies that the entire integrated circuit (IC) of the shunt reference operates in parallel with its load (Figure 2). With a shunt voltage reference, you apply an input voltage to the resistor that connects to the cathode. The typical initial voltage accuracy of this device can range from 0.5 to 5 percent, with a temperature coefficient of approximately 50 to 100 µV/°C. The shunt voltage reference is appropriate for converters with less than 8 bits.

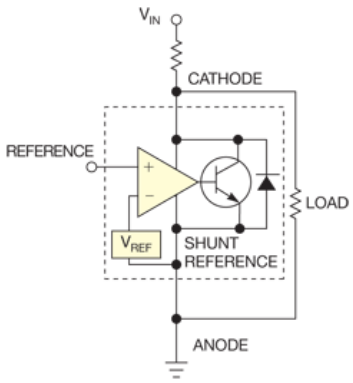

Figure 2: The two-terminal shunt voltage reference implies that the entire IC chip of the shunt reference operates in parallel with its load.

The series-voltage reference operates in series with its load (Figure 3). An internal bandgap voltage, in combination with an internal amplifier, creates the output voltage of this reference. The series-voltage reference produces an output voltage between the output and ground and provides the appropriate output current to the external load. As the load current increases or decreases, the series reference maintains the voltage at V_{OUT}.

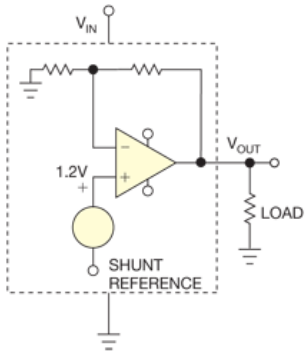

Figure 3: The series voltage reference operates in series with its load.

The typical initial voltage accuracy of a series reference can range from 0.05 to 0.5 percent, with temperature coefficients as high as 2.5 ppm/°C. Because of the series reference's superior initial voltage and over temperature performance, you can use this type of device when driving the reference pins of precision ADCs and digital-to-analog converters (DACs). Beyond 8-bit resolution where the least-significant bit (LSB) size is 0.39 percent, or 14 where the LSB size is 0.006 percent, an external series-voltage reference ensures that you can achieve the intended precision with your data converter.

References

1. Baker, Bonnie. How voltage references affect mixed-signal parts. EDN: Aug 26, 2010.

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6. Go for the gold with voltage-reference circuits

High-resolution mixed-signal devices present an interesting challenge as you try to find the right voltage reference design. Although no universal approach exists for these voltage-reference designs, the circuit in Figure 1 presents an interesting approach for greater-than-15-bit analog-to-digital converters (ADCs).

Some design issues of concern with high-resolution data converters are voltage-reference noise, stability and the reference circuit's ability to drive the voltage-reference pin of your data converter. The passive filter comprising R_1, C_2 and C_3 dramatically reduces the voltage-reference noise. The corner frequency of this low-pass filter is 1.59 Hz. This filter reduces both broadband and extremely low-frequency noise. The additional resistor/capacitor (RC) filter brings the noise level under control enough for a 20-bit ADC; an encouraging situation. However, if current is pulled through R_1 from the

ADC's reference pin, the voltage drop will corrupt the conversion by introducing a voltage drop with each bit decision (Reference 1).

The circuit diagram in Figure 1 has an operational amplifier (op amp) to isolate the low-pass filter comprising R_1, C_2 and C_3 and to provide adequate drive to the ADC's reference pin. The input bias current of the OPA350 CMOS op amp is 10 pA at 25°C. This current combines with R_1's resistance of 10 kΩ to generate a constant 100-nV DC drop. This level of voltage drop does not change a 23-bit ADC's final bit decision. The input bias current of the op amp changes over temperature, but you can expect a maximum current that is no more than 10 nA at 125°C, generating a change of 100 µV over a 100°C temperature range.

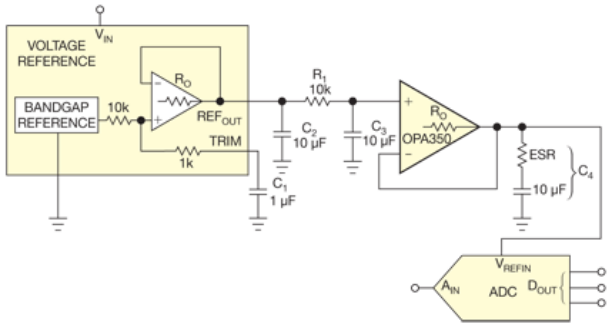

Figure 1: Although no universal approach exists for these voltage-reference designs, this circuit presents an interesting approach for converters with greater than 15 bits of resolution.

It is useful to put the voltage drop across R_1 into perspective. This voltage drop adds to the errors of the voltage-reference device. Suppose that the initial error of the voltage-reference circuit is ±0.05 percent with an error over temperature of 3 ppm/°C. With a reference of 4.096 V, the initial voltage-reference error is equal to 2.05 µV at room temperature, plus 1.23 µV at 125°C. In the circuit shown in Figure 1, the voltage-reference device dominates over the op amp's offset and input bias-current errors. An ADC that connects to the circuit in Figure 1 provides the summation of errors from the voltage reference, R_1, and OPA350 as a gain error.

The op amp drives a 10-µF capacitor, C_4, and the ADC's voltage-reference input pin. The charge residing on C_4 provides the needed charge during the ADC's conversion. During the ADC's acquisition and conversion, the size of C_4 provides a stiff voltage reference for the ADC's reference pin, which usually has an input capacitance of approximately 2 to 50 pF.

You can compromise the op amp's stability because C_4 and the op amp's open-loop output resistance, R_O, modify the op amp's open-loop gain curve. Basically, a circuit with good stability is one in which both the modified op amp's open-loop-gain curve and the closed-loop voltage-gain curve's rate of closure is 20 dB (Figure 2).

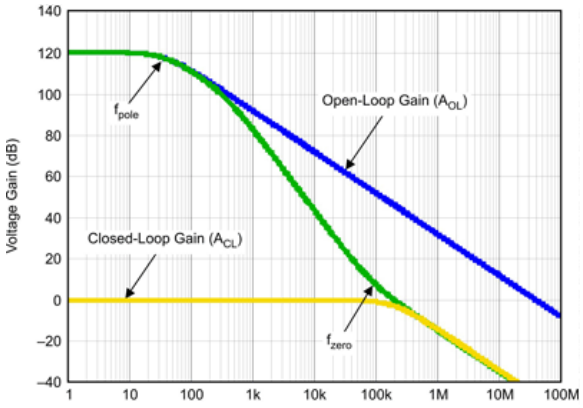

Figure 2: A circuit with good stability is one in which the modified op amp's open-loop-gain curve and the closed-loop voltage-gain curve's rate of closure is 20 dB.

In this stable circuit, Equations 1 and 2 calculate the frequency locations of the pole and zero:

$$f_P = \frac{1}{2 \times \pi \times (R_O + R_{ESR-C4}) \times C_4} = 318 \text{ Hz};$$

$$f_Z = \frac{1}{2 \times \pi \times R_{ESR-C4} \times C_4} = 78 \text{ kHz}.$$

(1, 2)

The open-loop output resistance of the OPA350 is 50 Ω and the equivalent series resistance (ESR) of C_4 is 2 mΩ.

References

1. Baker, Bonnie. Taking the mixed-signal voltage reference to a higher level. EDN: Sept 23, 2010.
2. Baker, Bonnie. Just use a 100 Ω resistor. EDN: Nov 27, 2008.
3. OPA350 datasheet.

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7. From high to low frequencies with IBIS

One challenge that high-speed digital-system designers have is tackling overshoot, undershoot, mismatched-impedance ringing, jitter distribution and cross-talk problems on their printed circuit boards (PCBs). These problems fall into the category of signal integrity. Many high-speed system designers use the input/output buffer information specification (IBIS) modeling language to anticipate and solve signal-integrity problems. This modeling language has been around since the early 1990s and has evolved into a formal standard: EIA-ANSI 656-B. The standard is alive and well, and the IBIS Consortium released version 6 in September 2013. IBIS uses current-to-voltage (I-V) and voltage-to-time (V-t) data tables to describe a device's input/output (I/O) pin characteristics. Manufacturers generate these tables by simulating or measuring their devices' I/O cells.

This type of simulation tool is necessary for high-speed designs that are now stretching up to clock rates as high as 10 Gbps. IBIS simulation times are considerably shorter than those of simulation program with integrated circuit emphasis (SPICE), and the results are equally accurate. It takes days or weeks for a large PCB system to complete a transistor-level SPICE simulation, whereas an IBIS simulation takes minutes or hours to execute. From an IBIS simulation, you can generate transmission-line responses and eye diagrams.

Customers are now asking for IBIS support with lower-frequency devices, with clocks that operate at frequencies lower than 40 MHz. Even at the lower frequencies, digital-signal edge rates cause signal-integrity issues. These fast edge rates can be responsible for clock signals that ring, causing a misinterpretation of a command or even an unexpected gain of two from an analog-to-digital converter (ADC). Integrated circuit (IC) manufacturers have sophisticated analog SPICE macro models for precision devices, but they are just catching up with the IBIS digital I/O-model library. Figure 1 illustrates an example in which an IBIS-model simulation would be useful.

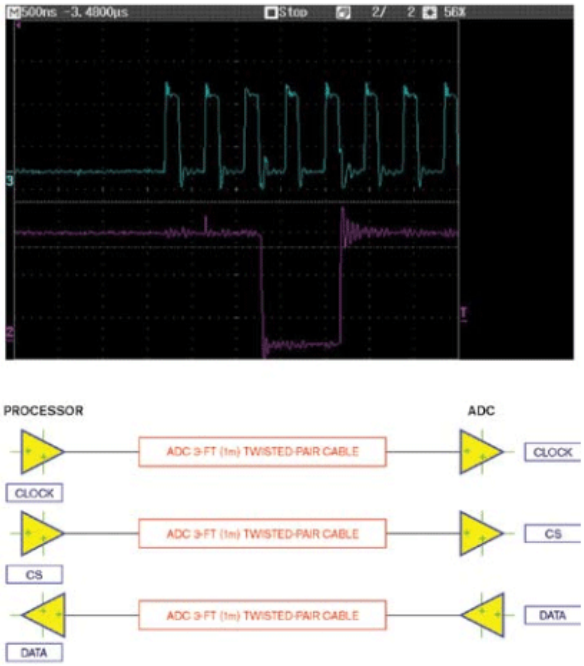

Figure 1: An IBIS simulation would be useful in this example, in which the clock- and data-signal termination method creates signals that exceed specified high- and low-level thresholds.

In this circuit, the designer has not paid attention to line impedances. Figure 1 shows the measured results of an ADC in the system. The ADC and processor reside on their respective boards, and the designer simply connected the two boards together through 1-meter category 5 twisted-pair cables. The frequency of the clock signal from the processor is 2.25 MHz (CH3). The ADC uses this signal to synchronize the transmission of data back to the processor (CH2).

Initially, the designer thought that the low clock speed between these two devices would not cause termination problems. However, the termination used in this circuit creates signals that exceed high and low thresholds, causing ringing and degraded eye diagrams. IBIS simulations to the rescue! Save time and reduce costs. Identify problem digital circuits before turning your circuit into hardware.

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3. Using IBIS models for timing analysis. Texas Instruments Application Report SPRA839, April 15, 2003.
4. ANSI/EIA-656-B I/O Buffer Information Specification (IBIS), Version 4.2.

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Bonnie Baker is a Senior Applications Engineer with the WEBENCH® team for Texas Instruments and has been involved with analog and digital designs and systems for over 25 years. In addition to her fascination with circuit design, Bonnie has a drive to share her knowledge and experience. She has written hundreds of articles, design and application notes, conference papers, articles, including a monthly column in EDN magazine and on edn.com called "Baker's Best." Additionally, Bonnie has authored a book: "A Baker's Dozen: Real Analog Solutions for Digital Designers." Check out her latest blog, On Board with Bonnie, where she navigates the ins and outs of signal chain designs.

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